

ELx35 interface description



Described product

ELx35 Interface description

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1 General description

This specification describes the ELS/ELM35 interface including register settings, error and warning description and general commands.

2 Basics

- BiSS-C protocol
- Point-to-point configuration with only one connected sensor (only one sensor data channel: encoder position).
- Sensor data format according to BiSS-C Profile 3 (BP3) for Rotary and Linear encoder.
- Maximal Master clock frequency: 10 MHz (maximal possible MA frequency in the application depends on cable length).

3 Sensor data format

During normal operation the encoder outputs the position in a BP3 format:

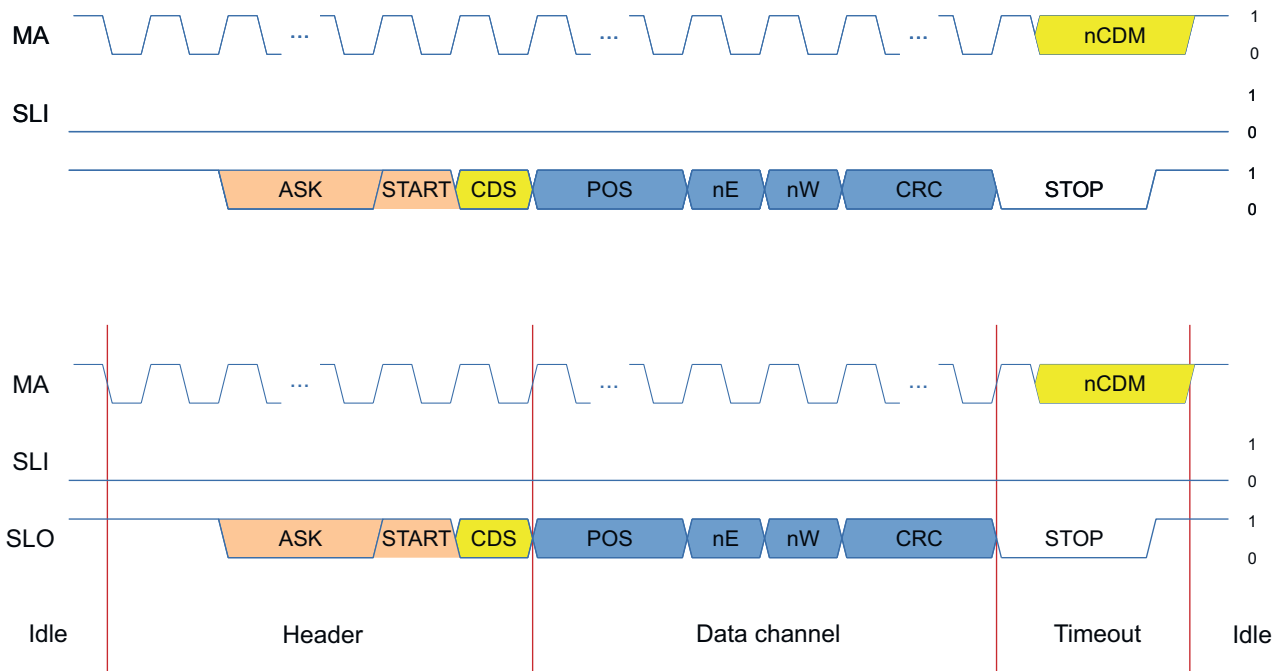


Figure 1: Sensor data format

- ① “Header” consist of following bits: Ack /Start / CDS
- ② “MT & ST” (Multiturn & Singleturn Position)
- ③ “nE & nW” Error bit and Warning bit (is set to “0” in case of an error/warning)
- ④ “CRC” 6 bit checksum to secure the data channel
- ⑤ “Timeout” indicates the end of the BiSS frame.

4 Sensor Data Format Definition

BiSS-C frame / Data format definition (BP3 format):

Processing time is about 2~3us.

MT (Multiturn resolution in bits):

- ELS35 (Single-Encoder): MT = 0 bits
- ELM35 (Multi-Encoder): MT = 12 bits

ST (Singleturn resolution in bits):

- ELS35 (Single-Encoder): ST = 24 bits
- ELM35 (Multi-Encoder): ST = 24 bits

nE: Error bit is set to “0” in case of an error bit is set in status register (0x72)

nW: Warning bit is set to “0” in case of a warning bit is set in status register (0x70)

CRC: 6 bit CRC value is calculated over [MT+ST+nE+nW] bits

- Calculation: CRC polynomial: $0x43 = X^6 + X^1 + X^0$ CRC start value: 0x00

Timeout: The length of the timeout is about 1.5 MA clock (adaptive timeout)

Max Biss frame frequency: 50 KHZ (20us data cycle) depending on MA frequency.

5 BiSS-C Slave Register

Register Addr. 0x00..0x3F is accessed via bank assignment.

The table below shows the memory banks open to user.

Table 1: Memory banks

| Bank Number | Name | Size | R/W | Memory |
|-------------|-------------------|------------|-----|--------|
| 0x00..0x1F | User data memory | 2048 bytes | R/W | E2P |
| 0x62 | EDS Common Part | 64 bytes | R | E2P |
| 0x63 | EDS Biss BP3 part | 64 bytes | R | E2P |



NOTE

After writing to User data memory, execute command 0x08 (CHKSUM_CALCULATION) to update E2P CHKSUM. The last 4 bytes of the user data memory is reserved for storage of user data CHKSUM.

Following table shows all supported slave registers, which can be directly accessed by the BiSS-C control communication (without bank selection).

Table 2: Supported slave registers

| Addr. | Name | Size | R/W | Memory |
|------------|--|---------|-----|--------|
| 0x40 | Bank selection | 1 byte | R/W | RAM |
| 0x41 | EDS bank - 0x62 | 1 byte | R | E2P |
| 0x42 | Profile ID – 0x62 (BP3) | 1 byte | R | E2P |
| 0x43 | Profile ID – Data Length + 2 | 1 byte | R | E2P |
| 0x44..0x4C | Serial number: YY (2 byte) - WW (2 byte) - xxxx (4 bytes) - “V” (1 byte) (ASCII for all byte) | 9 bytes | R | E2P |
| 0x4D..0x4F | ¹⁾ Offset ST Position (Big Endian, by default Zero) | 3 bytes | R | E2P |
| 0x50..0x51 | ¹⁾ Offset MT Position (Big Endian, by default zero) | 2 bytes | R | E2P |

| Addr. | Name | Size | R/W | Memory |
|------------|--|----------|-----|--------|
| 0x52..0x53 | Encoder voltage supply value in 0.1 V saved as a Big Endian | 2 bytes | R | RAM |
| 0x54..0x55 | Internal temperature sensor reading in 0.1 °C as a Big Endian | 2 bytes | R | RAM |
| 0x56..0x58 | ²⁾ Preset ST Position (Big Endian, by default Zero) | 3 bytes | R/W | E2P |
| 0x59..0x5A | ²⁾ Preset MT Position (Big Endian, by default zero) | 2 bytes | R/W | E2P |
| 0x5B | Reserved | 1 byte | R/W | E2P |
| 0x5C | Reserved | 1 byte | R/W | E2P |
| 0x5D..0x5E | Median Speed recorded during motor integration test (in RPM as a Big Endian, minus value indicate CCW) | 2 bytes | R | RAM |
| 0x5F | Speed deviation recorded during motor integration test (max - min) (in RPM) | 1 byte | R | RAM |
| 0x60..0x6F | Reserved for system use | 16 bytes | - | - |
| 0x70..0x71 | Status Register (Warning) | 2 bytes | R | RAM |
| 0x72..0x73 | Status Register (Error) | 2 bytes | R | RAM |
| 0x74 | Command Register | 1 byte | R/W | RAM |
| 0x75 | Command argument (default 00) | 1 byte | R/W | RAM |
| 0x76 | Type of encoder: X (ASCII for "S" or "M") | 1 byte | R | E2P |
| 0x77..0x7D | Device ID: XXXXXX (7x ASCII for part number) | 7 bytes | R | E2P |
| 0x7E..0x7F | Manufacture ID - 0x53 0x53 (ASCII for "S S") | 2 bytes | R | E2P |

- 1) The Offset position is read only, which indicates User PRESET Command executed. RESET command will set the two registers to default zero again.
- 2) Encoder output position will be set to Preset value during PRESET command. For ST, the value is in the form of 24 bits resolution per turn. For example, 0x40 00 00 represent 90 mechanical degrees.

6 Status Register for Warning

Table 3: Status Register for Warning


| Addr. | Name | Comments |
|-------|--|---|
| 0x70 | *Bit 0: Warning: Temperature critical *Bit 1: Warning: Voltage supply critical Bit 2: Warning: Calibration failure Bit 3: Warning: Speed fluctuation out of range Bit 4: Warning: Bit 5: Warning: BiSS-C Command not valid *Bit 6: Warning: Command execution active Bit 7: Warning: Internal communication not valid | Indicate temperature out of range (-25° ..105 °C by default) Indicate voltage supply out of range (4.5..5.5 V by default) Indicate calibration not successful in factory Indicate speed fluctuation exceed during motor test - Indicate command written to register 0x74 not defined Indicate command in execution Indicate internal communication error (for debugging) |
| 0x71 | Reserved for future use | |

- * Bit 0, 1, 6 are non-sticky. Other Bits are sticky, and will be cleared by SCLEAR command, RESET command or power Cycle.

7 Status Register for Error

Table 4: Status Register for Error

| Addr. | Name | Comments |
|-------|--|---|
| 0x72 | Bit 0: Error: Position Error Bit 1: Error: Synchronization Error Bit 2: Error: Sync over limit Bit 3: Error: Bit 4: Error: Bit 5: Error: Error: FCT Error Bit 6: Error: Initialization Error Bit 7: Error: EEPROM error | Indicate position sensing not reliable with high disturbance Indicate absolute position generation error Indicate absolute position generation not reliable - - Indicate PCBA error during FCT testing Indicate internal configuration error during start-up Indicate EEPROM error during start-up |
| 0x73 | Reserved for future use | |

 **NOTE**
 All error Bits indicate critical issue with encoder and position output is not reliable. System should react immediately to stop operation.
 All error Bits are sticky and cannot be cleared with SCLEAR command. Use RESET command or Power Cycle to clear the error Bits.

8 General command

General Command can be executed by a write access on register 0x74.

Table 5: General command

| Addr. | Command Value | Argument value | Name |
|-------|---------------|----------------|------------------------------|
| 0x74 | 0x00 | - | NO COMMAND |
| | 0x01 | - | RESET |
| | 0x02 | - | SETPOS_ST |
| | 0x03 | - | SETPOS_MT |
| | 0x23 | - | SETPOS_ST_MT |
| | 0x04 | - | FACRESET |
| | 0x05 | - | SCLEAR |
| | 0x06 | 0xXX | START_MOTOR_INTEGRATION_TEST |
| | 0x07 | - | STOP_MOTOR_INTEGRATION_TEST |
| | 0x08 | - | CHKSUM_CALCULATION |

RESET:

- Executes an encoder software reset. All parameters are newly initialized, and the absolute position is calculated new. All warning / Error status registers will be cleared after RESET. In case of a still active warning or error, the corresponding status bit will be set again.

SETPOS:

- Sets the encoder's output position to a preset value. This command must be executed in encoder standstill. During command execution the position output is invalid.

FACRESET:

- All registers value will be reset to factory default, including user data memory.

SCLEAR:

- Clears all warning status registers. In case of a still active warning, the corresponding warning bit will be set again after the status bit reset. Error status cannot be cleared by the SCLEAR command.

START_MOTOR_INTEGRATION_TEST:

- Execute this command after motor reach stable commanded speed. Encoder will check speed internally and record the fluctuation. The command argument indicates the allowed speed fluctuation value in RPM. If encoder detected higher fluctuation, BiSS-C Warning will be reported. Argument value is 0, which means no check on the fluctuation. (The speed fluctuation is measured with observation window 125 μ s by default). Additionally, during the command cycle, encoder conducts synchronization check as well. In case of failure, BiSS-C Error will be reported.

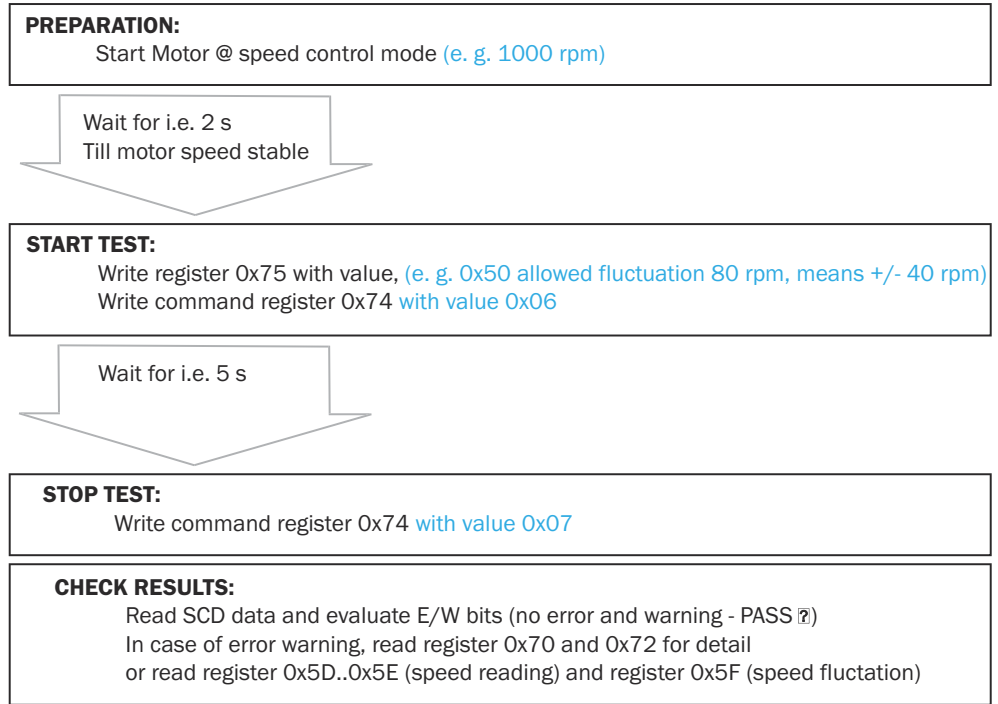
STOP_MOTOR_INTEGRATION_TEST:

- After execution of this command, controller may evaluate the test result from SCD E/W and BiSS-C register 0x5D ~ 0x5F.

CHKSUM_CALCULATION:

- Execute this command after writing data to user data memory. The data will be protected for damage detection during next start-up.

9 MOTOR INTEGRATION TEST – Flow CHART



NOTE

The internal speed observation window is about 0.125 ms, which will contribute to speed fluctuation reading about +/-20 rpm due to noise. As the frequency is above 8 KHZ, the impact to actual motor speed is minor.

10 BiSS-C Slave Register (Accessible to USER 2)

To access the following registers the User2 passcode has to be written in Bank 0x68, register 0x12..0x15.

Table 6: BiSS-C Slave Register

| Bank | Addr. | Name | Size | R/W | Memory |
|--------|------------|---|---------|-----|--------|
| 0x66 | 0x00..0x01 | Temperature Lower Limits (in 0.1 °C as a Big Endian) Default 0xFF 06 (-25 °C) | 2 bytes | R/W | E2P |
| | 0x02..0x03 | Temperature Upper Limits (in 0.1 °C as a Big Endian) Default 0x04 1A (105 °C) | 2 bytes | R/W | E2P |
| | 0x04..0x05 | Voltage supply Lower Limits (in 0.1 V as a Big Endian) Default 0x00 2D (4.5 V) | 2 bytes | R/W | E2P |
| | 0x06..0x07 | Voltage supply Upper Limits (in 0.1 V as a Big Endian) Default 0x00 37 (5.5 V) | 2 bytes | R/W | E2P |
| | 0x24..0x25 | Hysteresis Correction (in arcsecond as a Big Endian) | 2 bytes | R/W | E2P |
| | 0x26..0x27 | Hysteresis (in arcsecond as a Big Endian) | 2 bytes | R/W | E2P |
| 0x68 | 0x12..0x15 | User2 passcode (20231202) | 4 bytes | R/W | E2P |
| Direct | 0x5B | POSITION OUTPUT OPTION: 0x00, default mode 0x01, Under planning 0x02, debouncing enable mode | 1 byte | R/W | E2P |
| Direct | 0x5C | LUT selection: 0x00, default (factory LUT enable) 0x02, user LUT enable (Under Planning) | 1 byte | R/W | E2P |

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